



VN920D-B5 VN920DSO

HIGH SIDE DRIVER

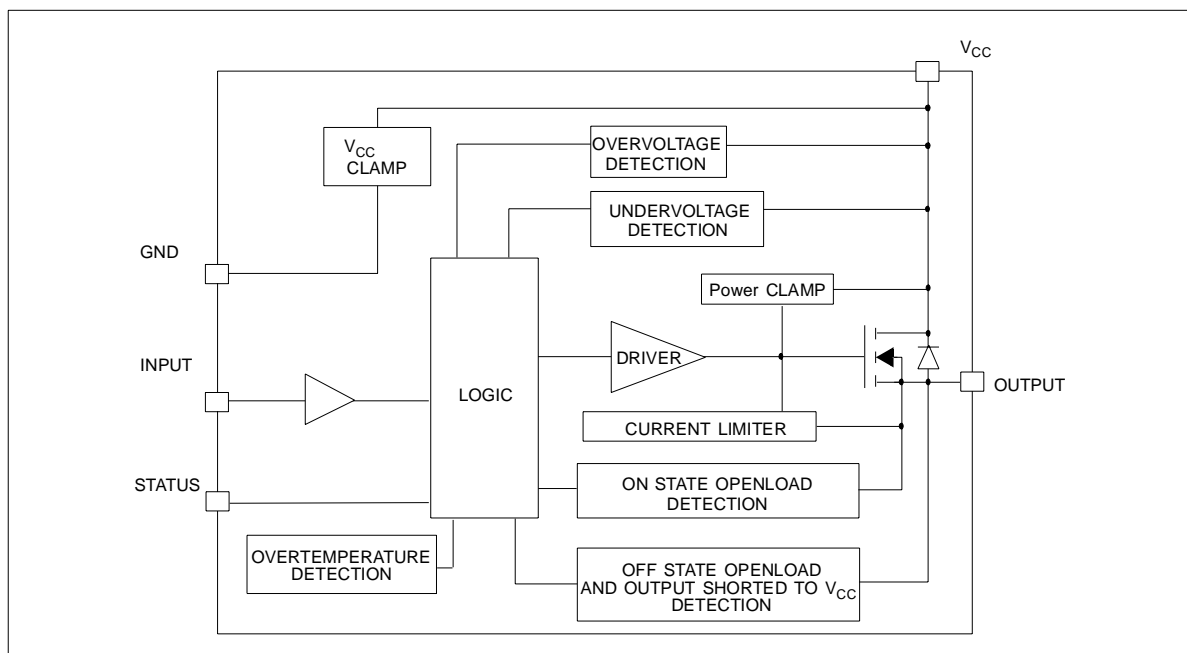
| TYPE | $R_{DS(on)}$ | I_{OUT} | V_{CC} |
|-----------|---------------|-----------|----------|
| VN920D-B5 | 18 m Ω | 30 A | 36 V |
| VN920DSO | | | |

- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (*)

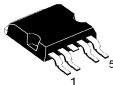
DESCRIPTION

The VN920D-B5, VN920DSO are monolithic devices made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637

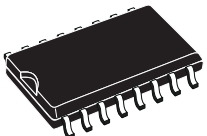
BLOCK DIAGRAM



(*) See application schematic at page 8



P²PAK



SO-16L

| ORDER CODES | | |
|--------------------|-----------|---------------|
| PACKAGE | TUBE | T&R |
| SO-16L | VN920DSO | VN920DSO13TR |
| P ² PAK | VN920D-B5 | VN920D-B513TR |

transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

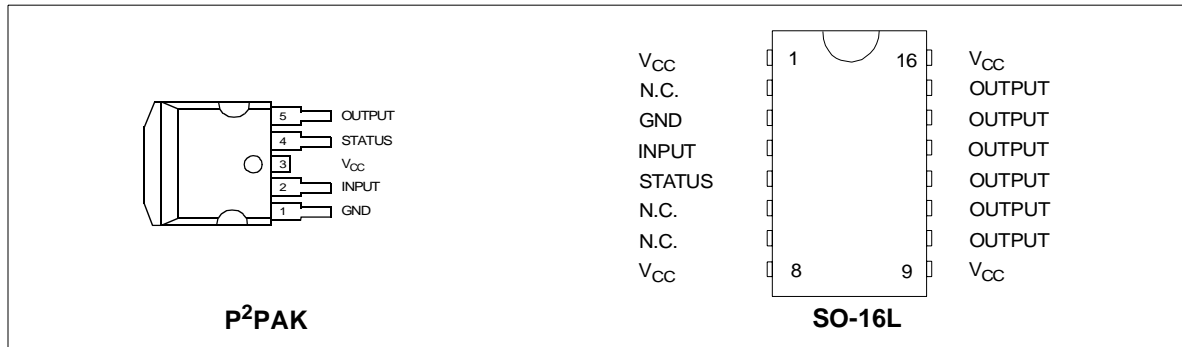
The device detects open load condition both is on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

VN920D-B5 / VN920DSO

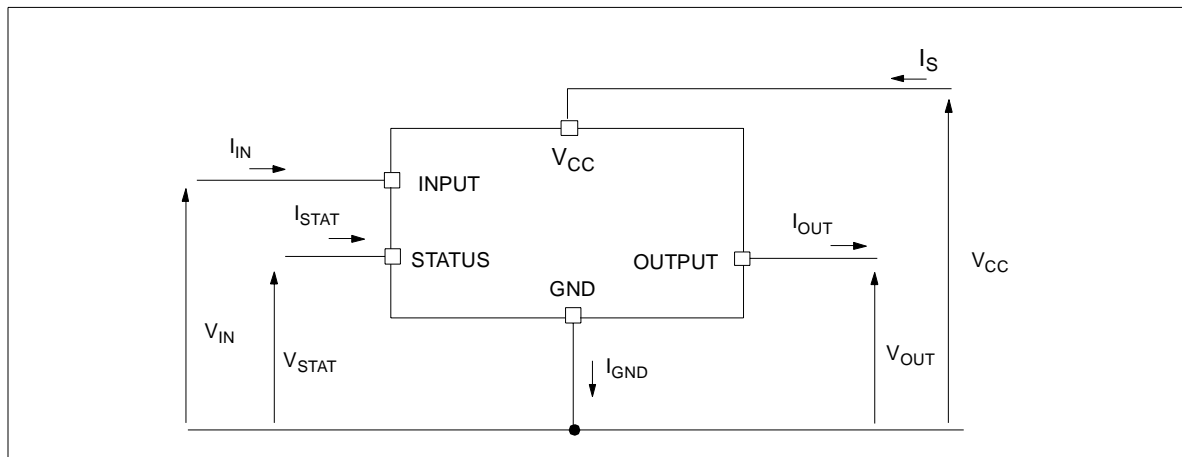
ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Value | | Unit |
|--------------------|--|--------------------|--------|------|
| | | P ² PAK | SO-16L | |
| V _{CC} | DC Supply Voltage | 41 | | V |
| - V _{CC} | Reverse DC Supply Voltage | - 0.3 | | V |
| - I _{GND} | DC Reverse Ground Pin Current | - 200 | | mA |
| I _{OUT} | DC Output Current | Internally Limited | | A |
| - I _{OUT} | Reverse DC Output Current | - 25 | | A |
| I _{IN} | DC Input Current | +/- 10 | | mA |
| I _{STAT} | DC Status Current | +/- 10 | | mA |
| V _{ESD} | Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) | | | |
| | - INPUT | 4000 | | V |
| | - CURRENT SENSE | 4000 | | V |
| | - OUTPUT | 5000 | | V |
| | - V _{CC} | 5000 | | V |
| E _{MAX} | Maximum Switching Energy (L=0.25mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =45A) | 364 | 352 | mJ |
| P _{tot} | Power Dissipation T _C =25°C | 96.1 | 8.3 | W |
| T _j | Junction Operating Temperature | Internally Limited | | °C |
| T _C | Case Operating Temperature | - 40 to 150 | | °C |
| T _{stg} | Storage Temperature | - 55 to 150 | | °C |

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

| Symbol | Parameter | | Value | | Unit |
|-----------------------|-------------------------------------|-----|--------------------|---------|------|
| | | | P ² PAK | SO-16L | |
| R _{thj-case} | Thermal Resistance Junction-case | Max | 1.3 | - | °C/W |
| R _{thj-lead} | Thermal Resistance Junction-lead | Max | - | 15 | °C/W |
| R _{thj-amb} | Thermal Resistance Junction-ambient | Max | 51.3 (*) | 65 (**) | °C/W |

(*) When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick).

(**) When mounted on FR4 printed circuit board with 0.5cm² of Cu (at least 35μ thick) connected to all V_{CC} pins.

ELECTRICAL CHARACTERISTICS (8V < V_{CC} < 36V; -40°C < T_j < 150°C unless otherwise specified)

POWER

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------------|-----------------------------------|--|-----|-----|-----|------|
| V _{CC} | Operating Supply Voltage | | 5.5 | 13 | 36 | V |
| V _{USD} | Undervoltage Shut-down | | 3 | 4 | 5.5 | V |
| V _{USDhyst} | Undervoltage Shut-down hysteresis | | | 0.5 | | V |
| V _{OV} | Overvoltage Shut-down | | 36 | | | V |
| R _{ON} | On State Resistance | I _{OUT} =10A; T _j =25°C | | | 18 | mΩ |
| | | I _{OUT} =10A | | | 36 | mΩ |
| | | I _{OUT} =3A; V _{CC} =6V | | | 50 | mΩ |
| I _S | Supply Current | Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V | | 10 | 25 | μA |
| | | Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C | | 10 | 20 | μA |
| | | On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A | | | 5 | mA |
| I _{L(off1)} | Off State Output Current | V _{IN} =V _{OUT} =0V | 0 | | 50 | μA |
| I _{L(off2)} | Off State Output Current | V _{IN} =0V; V _{OUT} =3.5V | -75 | | 0 | μA |
| I _{L(off3)} | Off State Output Current | V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C | | | 5 | μA |
| I _{L(off4)} | Off State Output Current | V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C | | | 3 | μA |

SWITCHING (V_{CC}=13V)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|------------------------|----------------------|-----|----------------------|-----|------|
| t _{d(on)} | Turn-on Delay Time | R _L =1.3Ω | | 50 | | μs |
| t _{d(off)} | Turn-off Delay Time | R _L =1.3Ω | | 50 | | μs |
| dV _{OUT} /dt _(on) | Turn-on Voltage Slope | R _L =1.3Ω | | See relative diagram | | V/μs |
| dV _{OUT} /dt _(off) | Turn-off Voltage Slope | R _L =1.3Ω | | See relative diagram | | V/μs |

INPUT PIN

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------------|--------------------------|------------------------|------|------|------|------|
| V _{IL} | Input Low Level | | | | 1.25 | V |
| I _{IL} | Low Level Input Current | V _{IN} =1.25V | 1 | | | μA |
| V _{IH} | Input High Level | | 3.25 | | | V |
| I _{IH} | High Level Input Current | V _{IN} =3.25V | | | 10 | μA |
| V _{I(hyst)} | Input Hysteresis Voltage | | 0.5 | | | V |
| V _{ICL} | Input Clamp Voltage | I _{IN} =1mA | 6 | 6.8 | 8 | V |
| | | I _{IN} =-1mA | | -0.7 | | V |

VN920D-B5 / VN920DSO

ELECTRICAL CHARACTERISTICS (continued)

STATUS PIN

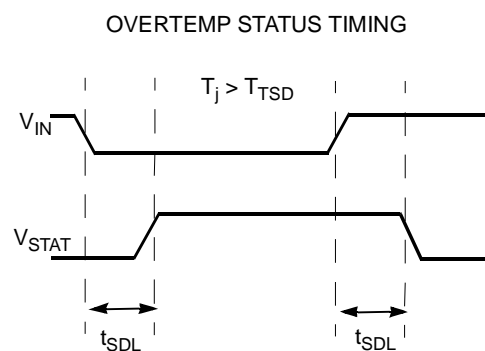
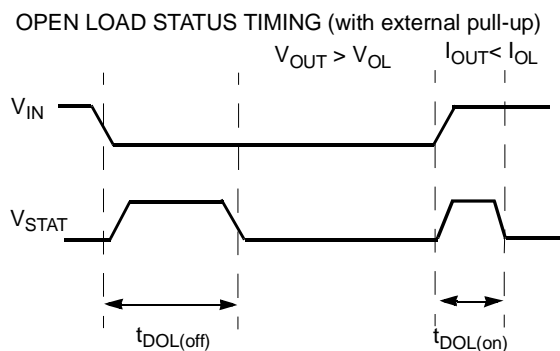
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------|------------------------------|--------------------------------|-----|------|-----|---------|
| V_{STAT} | Status Low Output Voltage | $I_{STAT}=1.6mA$ | | | 0.5 | V |
| I_{LSTAT} | Status Leakage Current | Normal Operation $V_{STAT}=5V$ | | | 10 | μA |
| C_{STAT} | Status Pin Input Capacitance | Normal Operation $V_{STAT}=5V$ | | | 100 | pF |
| V_{SCL} | Status Clamp Voltage | $I_{STAT}=1mA$ | 6 | 6.8 | 8 | V |
| | | $I_{STAT}=-1mA$ | | -0.7 | | V |

PROTECTIONS

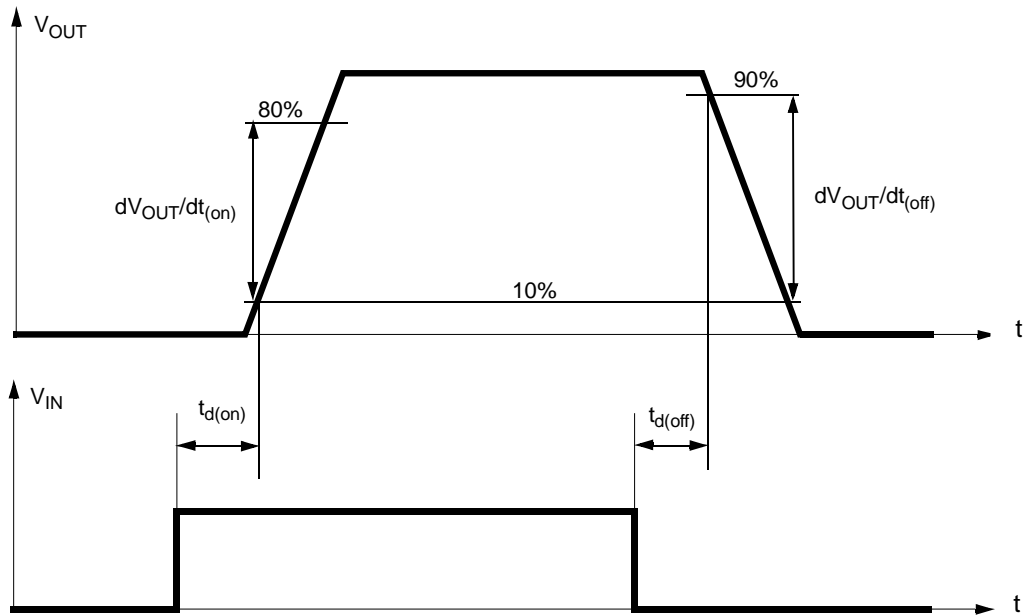
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------|------------------------------------|--------------------------------|-------------|-------------|-------------|-------------|
| T_{TSD} | Shut-down Temperature | | 150 | 175 | 200 | $^{\circ}C$ |
| T_R | Reset Temperature | | 135 | | | $^{\circ}C$ |
| T_{hyst} | Thermal Hysteresis | | 7 | 15 | | $^{\circ}C$ |
| t_{SDL} | Status delay in overload condition | $T_j > T_{TSD}$ | | | 20 | μs |
| I_{lim} | Current limitation | $5.5V < V_{CC} < 36V$ | 30 | 45 | 75 | A |
| V_{demag} | Turn-off Output Clamp Voltage | $I_{OUT}=2A; V_{IN}=0V; L=6mH$ | $V_{CC}-41$ | $V_{CC}-48$ | $V_{CC}-55$ | V |

OPENLOAD DETECTION

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------|--|-----------------|-----|-----|------|---------|
| I_{OL} | Openload ON State Detection Threshold | $V_{IN}=5V$ | 300 | 500 | 700 | mA |
| $t_{DOL(on)}$ | Openload ON State Detection Delay | $I_{OUT}=0A$ | | | 250 | μs |
| V_{OL} | Openload OFF State Voltage Detection Threshold | $V_{IN}=0V$ | 1.5 | 2.5 | 3.5 | V |
| $t_{DOL(off)}$ | Openload Detection Delay at Turn Off | | | | 1000 | μs |



Switching time Waveforms



TRUTH TABLE

| CONDITIONS | INPUT | OUTPUT | STATUS |
|---------------------------|-------|--------|---------------------|
| Normal Operation | L | L | H |
| | H | H | H |
| Current Limitation | L | L | H |
| | H | X | $(T_j < T_{TSD})$ H |
| | H | X | $(T_j > T_{TSD})$ L |
| Overtemperature | L | L | H |
| | H | L | L |
| Undervoltage | L | L | X |
| | H | L | X |
| Overvoltage | L | L | H |
| | H | L | H |
| Output Voltage $> V_{OL}$ | L | H | L |
| | H | H | H |
| Output Current $< I_{OL}$ | L | L | H |
| | H | H | L |

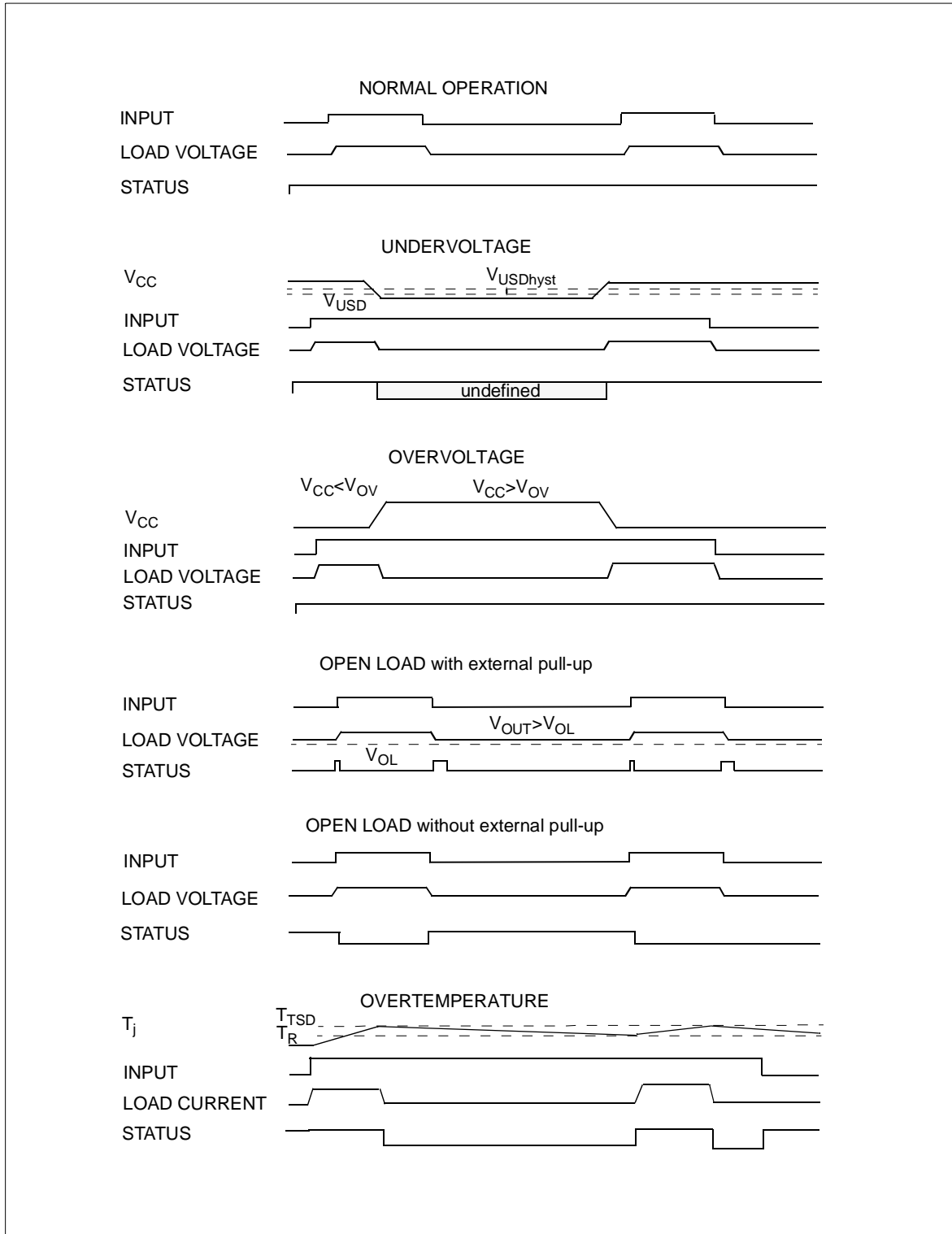
ELECTRICAL TRANSIENT REQUIREMENTS ON V_{CC} PIN

| ISO T/R 7637/1 Test Pulse | TEST LEVELS | | | | Delays and Impedance |
|------------------------------|-------------|---------|---------|---------|-------------------------|
| | I | II | III | IV | |
| 1 | -25 V | -50 V | -75 V | -100 V | 2 ms 10 Ω |
| 2 | +25 V | +50 V | +75 V | +100 V | 0.2 ms 10 Ω |
| 3a | -25 V | -50 V | -100 V | -150 V | 0.1 μs 50 Ω |
| 3b | +25 V | +50 V | +75 V | +100 V | 0.1 μs 50 Ω |
| 4 | -4 V | -5 V | -6 V | -7 V | 100 ms, 0.01 Ω |
| 5 | +26.5 V | +46.5 V | +66.5 V | +86.5 V | 400 ms, 2 Ω |

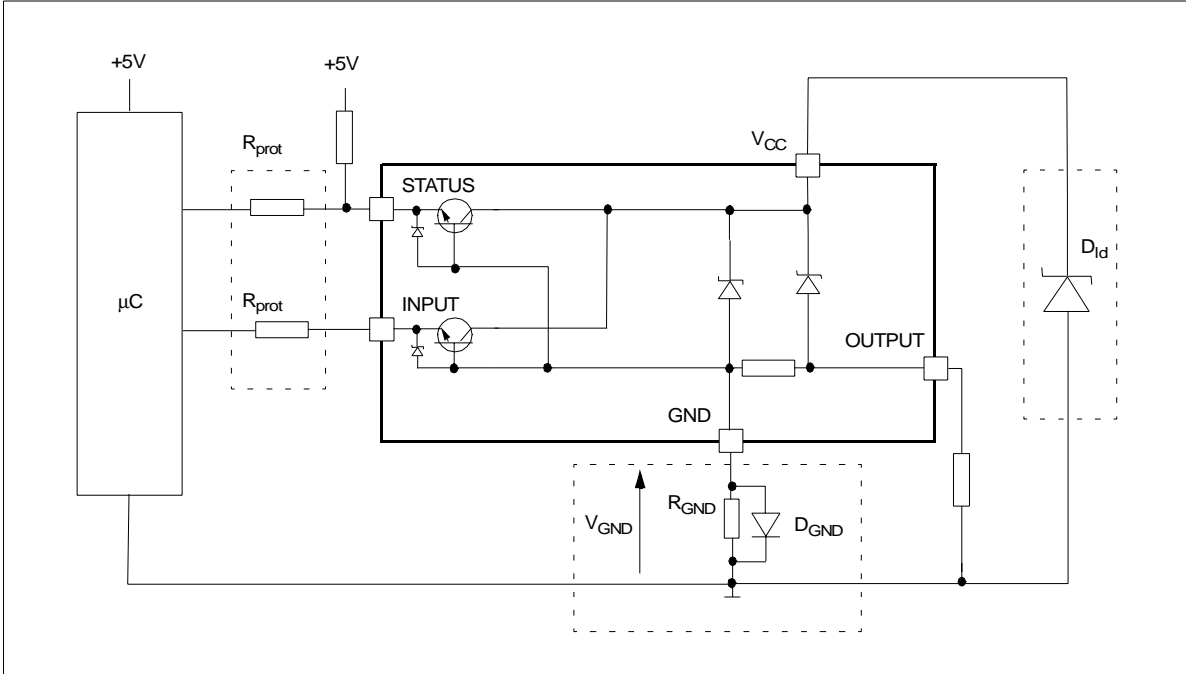
| ISO T/R 7637/1 Test Pulse | TEST LEVELS RESULTS | | | |
|------------------------------|---------------------|----|-----|----|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

| CLASS | CONTENTS |
|----------|---|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure1: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600mV / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggest to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OHµC} - V_{IH} - V_{GND}) / I_{IHmax}$$

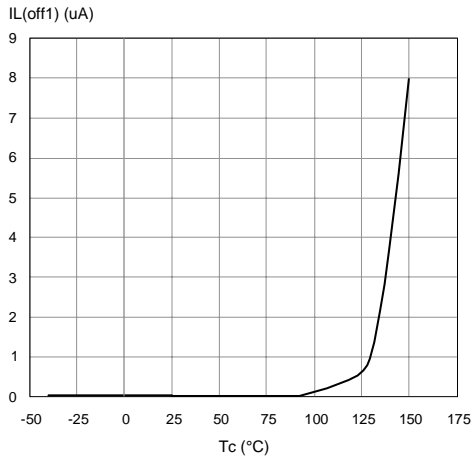
Calculation example:

For V_{CCpeak}= - 100V and I_{latchup} ≥ 20mA; V_{OHµC} ≥ 4.5V

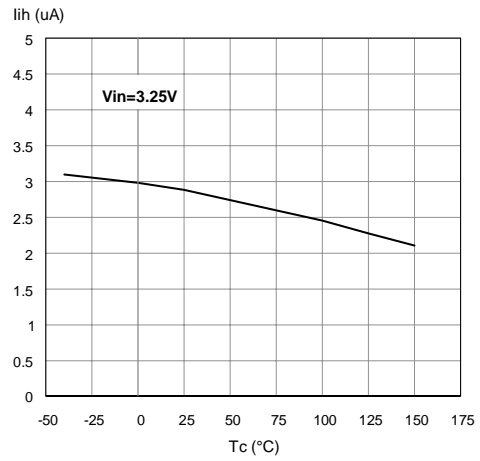
$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended R_{prot} value is 10kΩ.

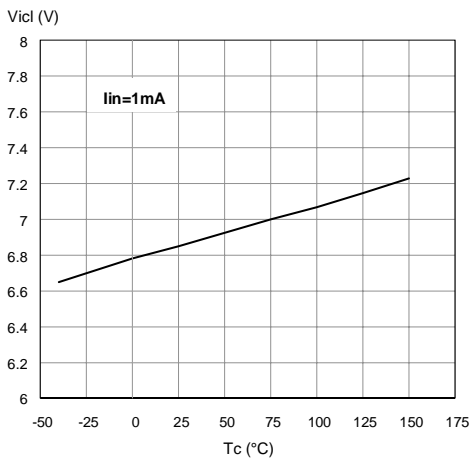
Off State Output Current



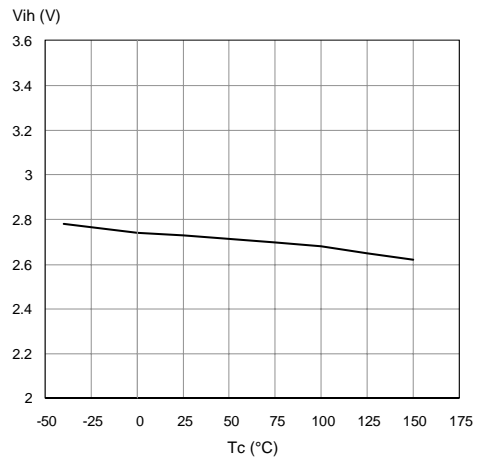
High Level Input Current



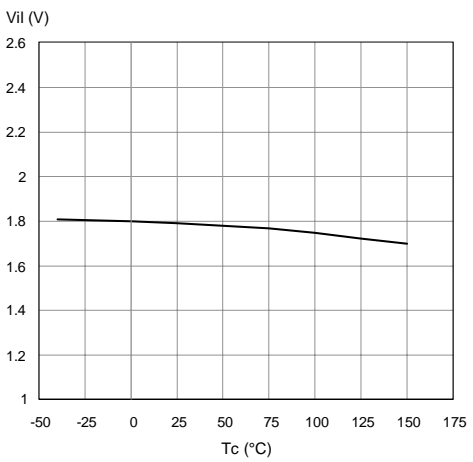
Input Clamp Voltage



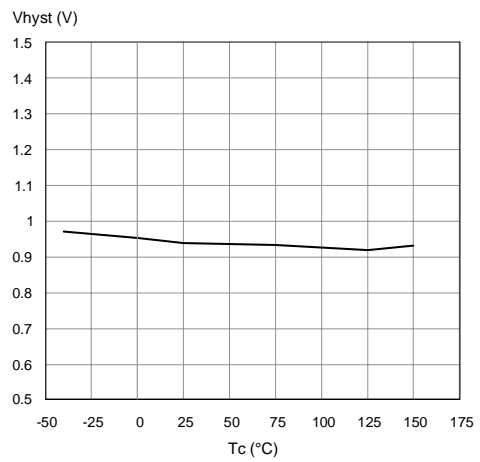
Input High Level



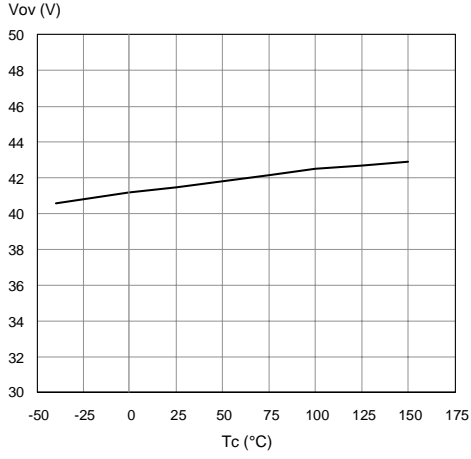
Input Low Level



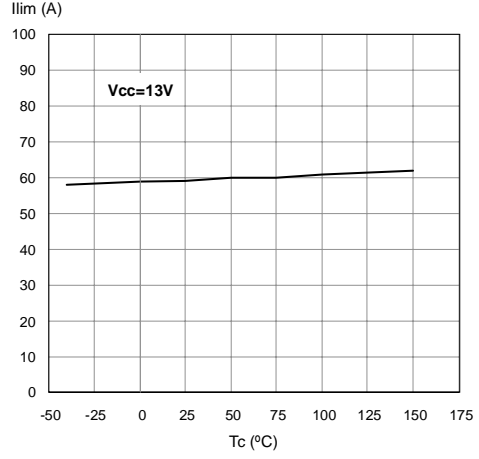
Input Hysteresis Voltage



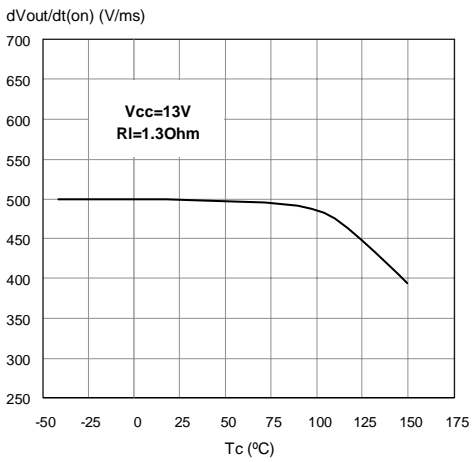
Overvoltage Shutdown



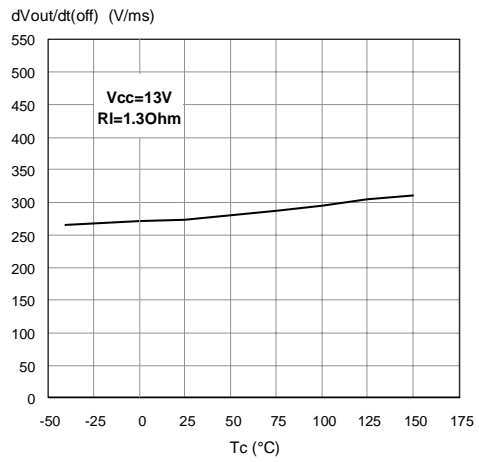
I_{LIM} Vs. T_{case}



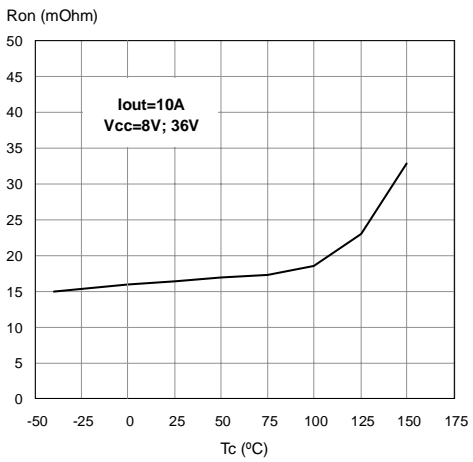
Turn-on Voltage Slope



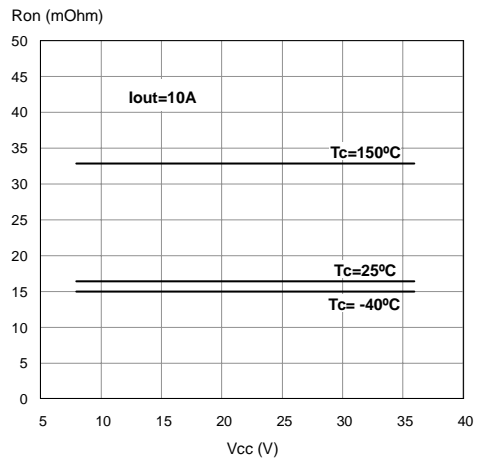
Turn-off Voltage Slope



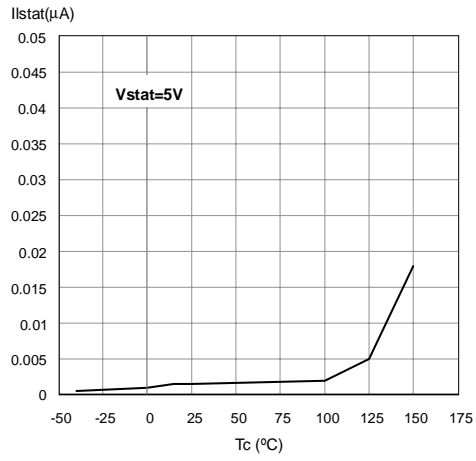
On State Resistance Vs. T_{case}



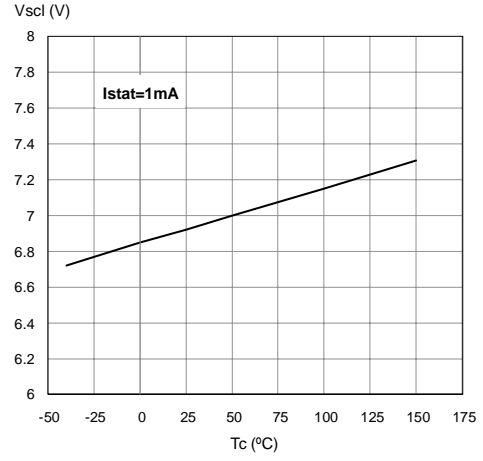
On State Resistance Vs. V_{CC}



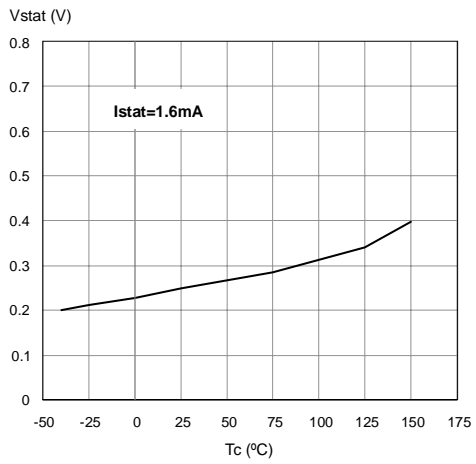
Status Leakage Current



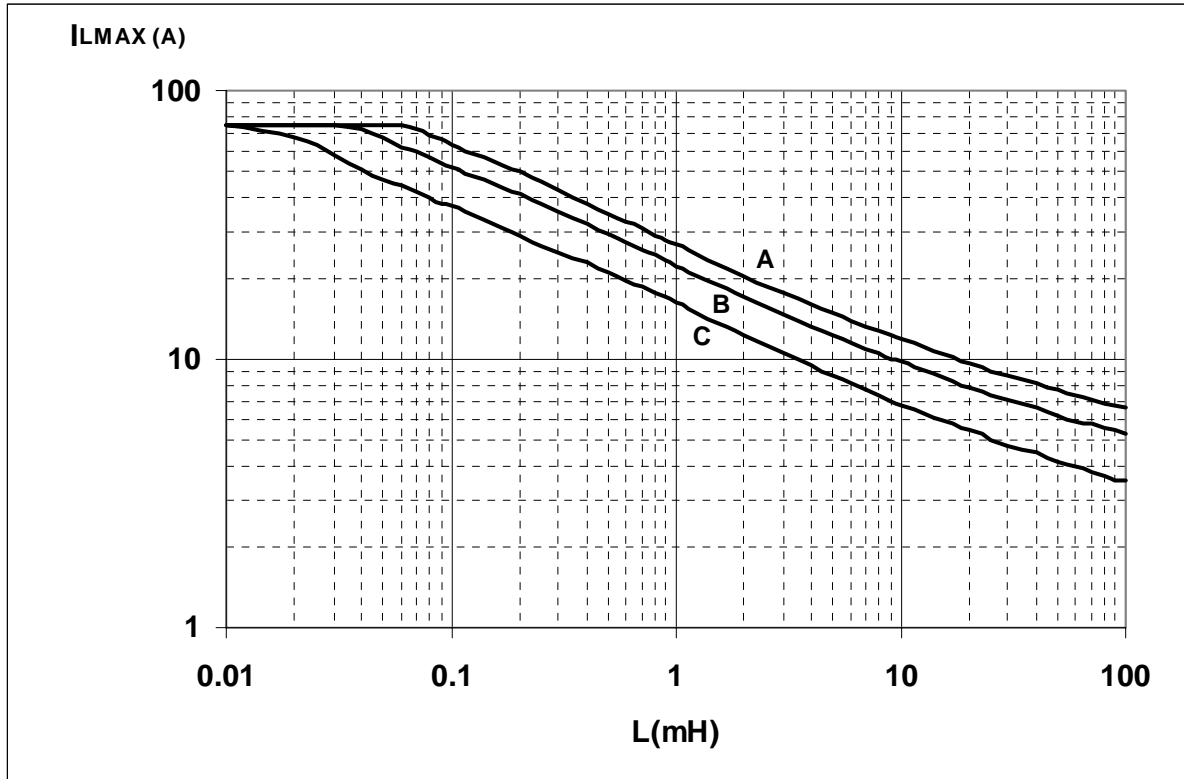
Status Clamp Voltage



Status Low Output Voltage



P²PAK Maximum turn off current versus load inductance



- A = Single Pulse at $T_{jstart}=150^{\circ}C$
- B = Repetitive pulse at $T_{jstart}=100^{\circ}C$
- C = Repetitive Pulse at $T_{jstart}=125^{\circ}C$

Conditions:

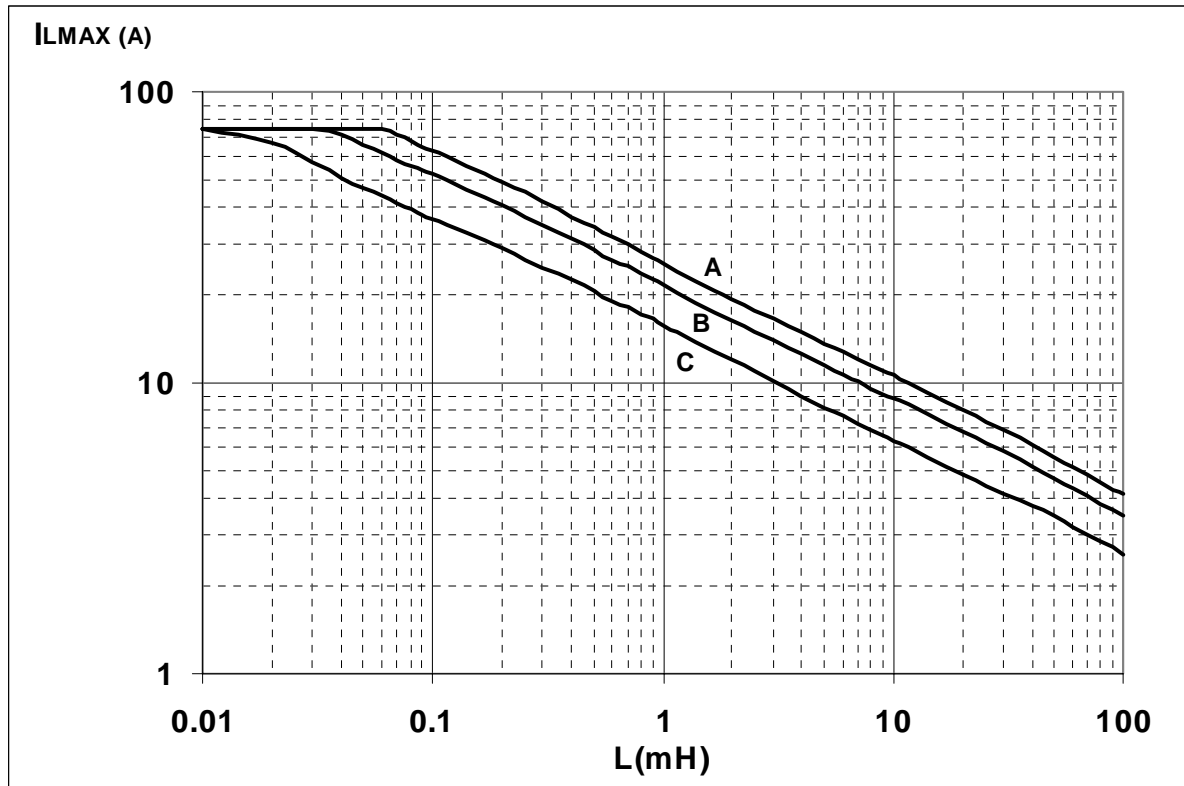
$V_{CC}=13.5V$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-16L Maximum turn off current versus load inductance



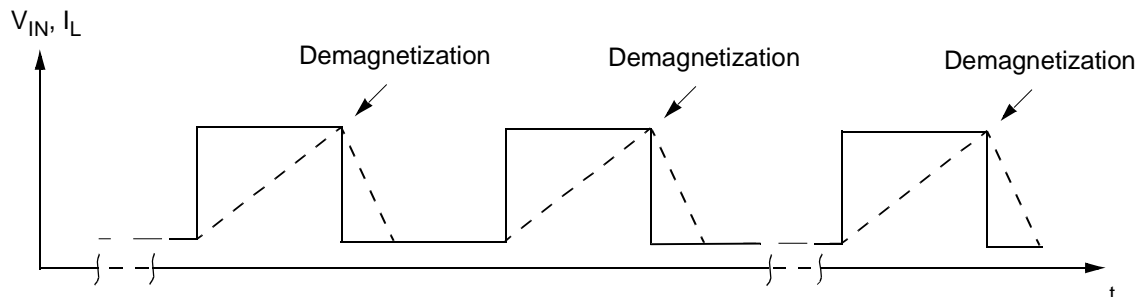
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

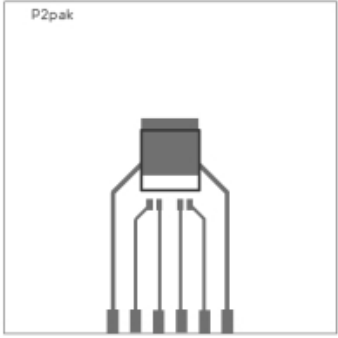
Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

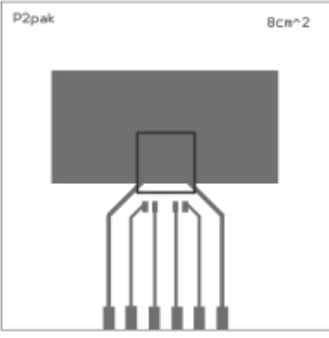


P²PAK THERMAL DATA

P²PAK PC Board



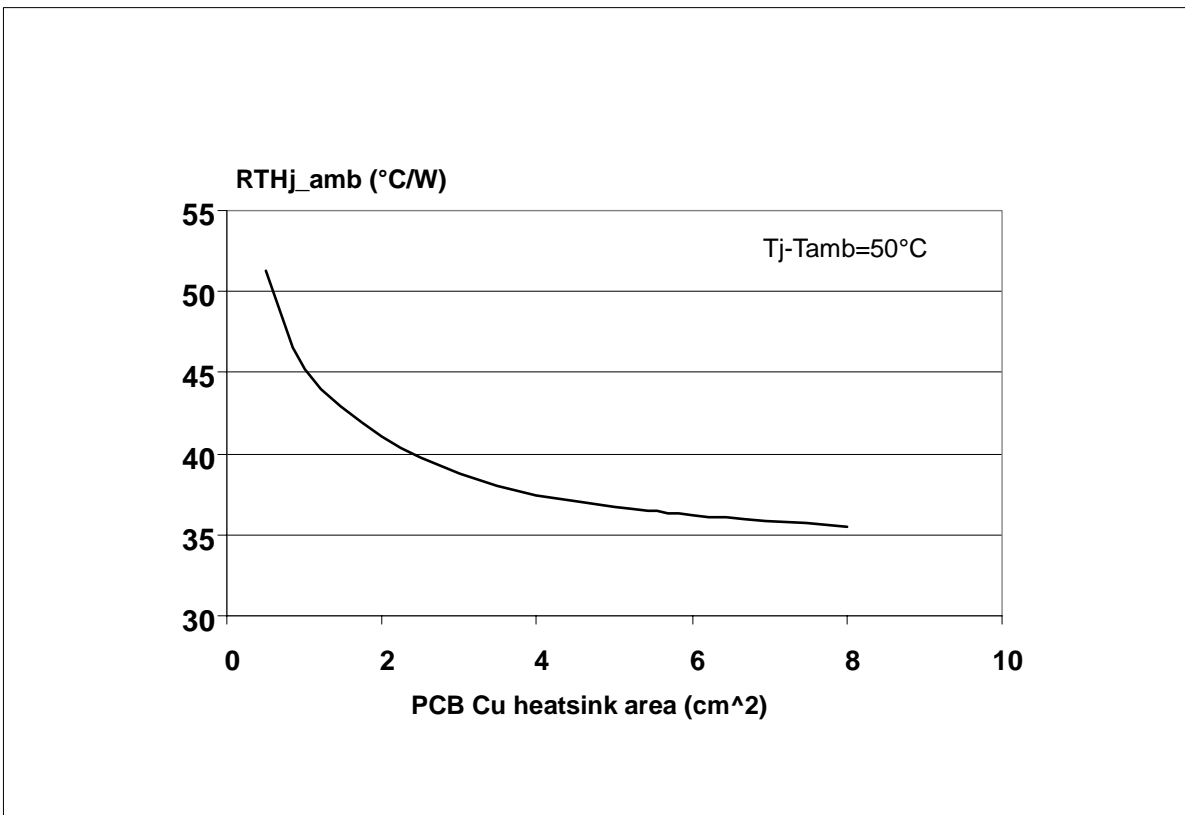
P2pak



P2pak 8cm²

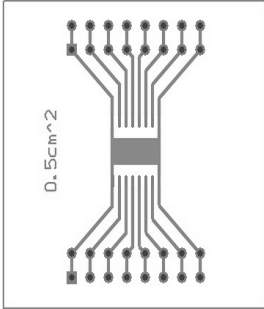
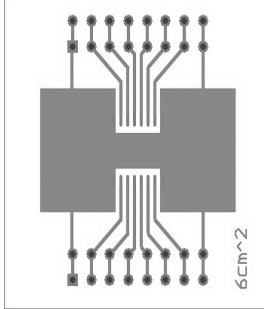
Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: 0.97cm², 8cm²).

$R_{thj-amb}$ Vs. PCB copper area in open box free air condition



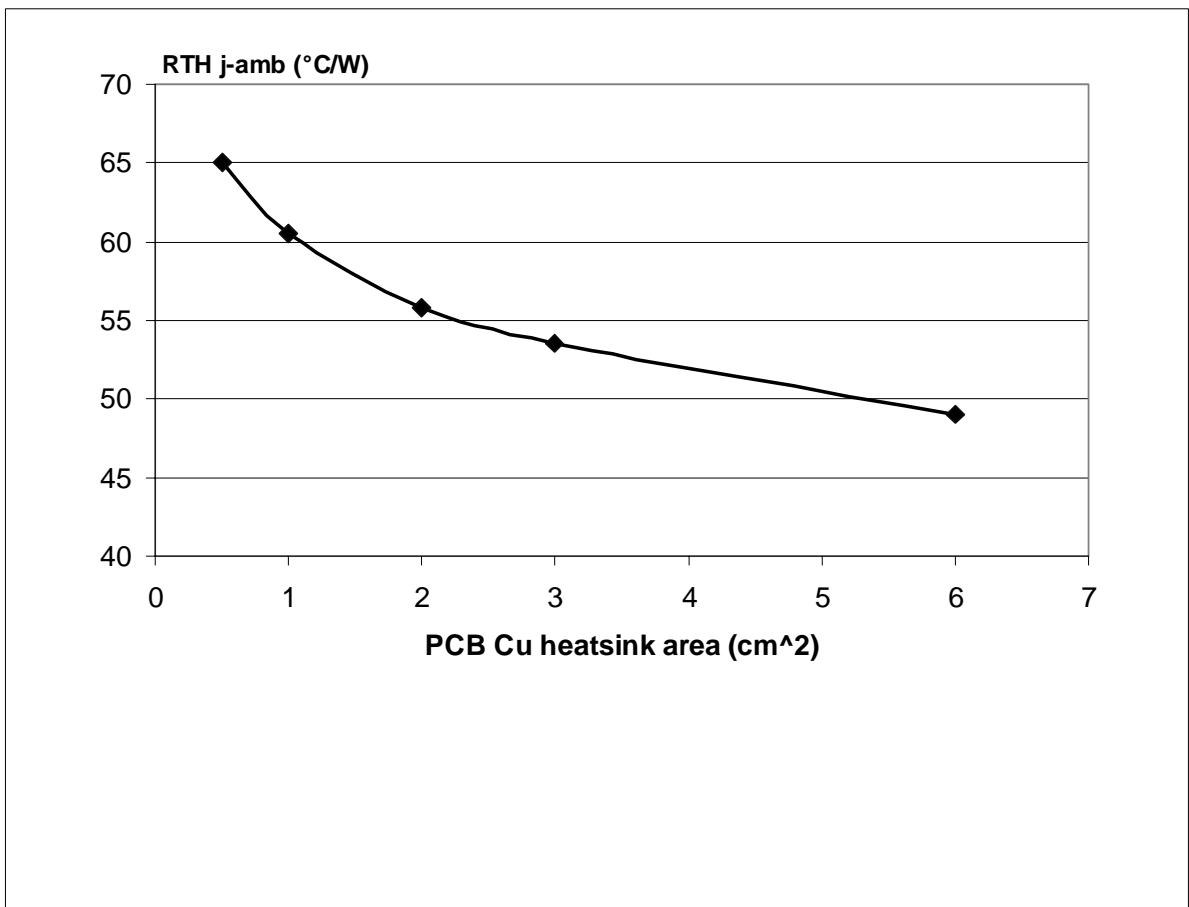
SO-16L THERMAL DATA

SO-16L PC Board

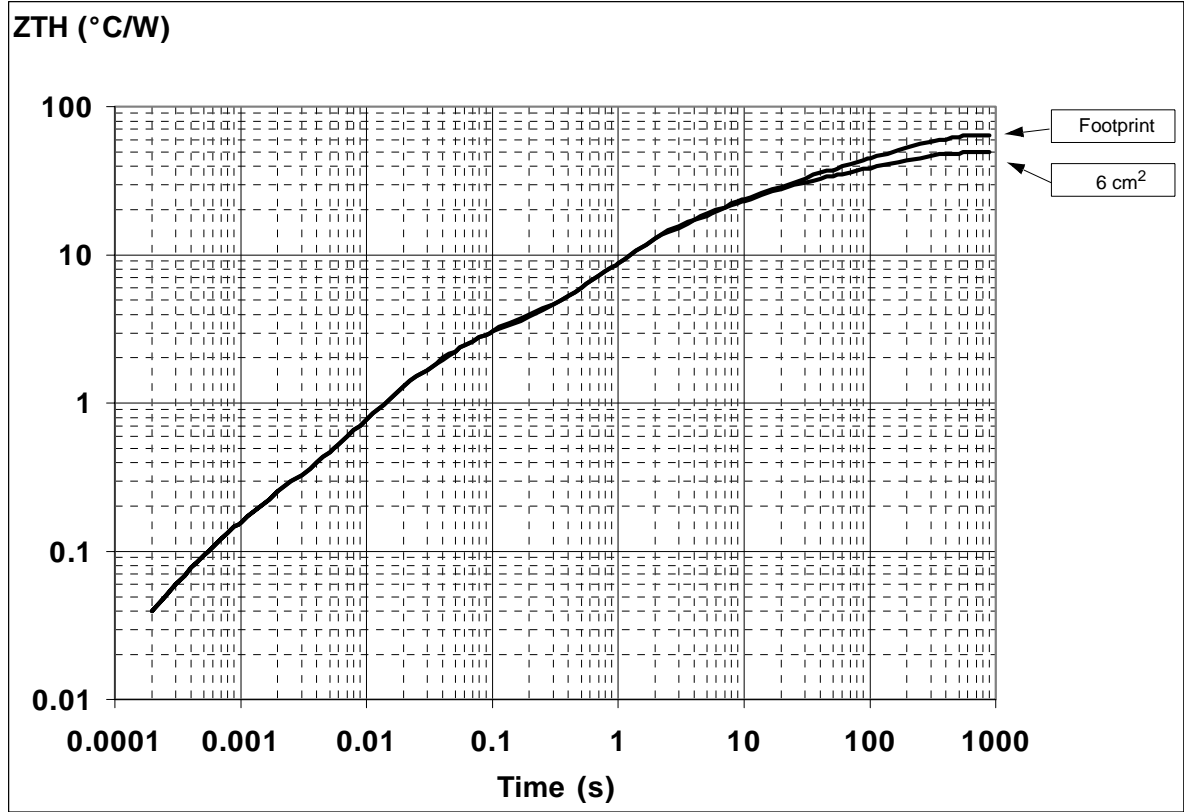



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 41mm x 48mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: 0.5cm², 6cm²).

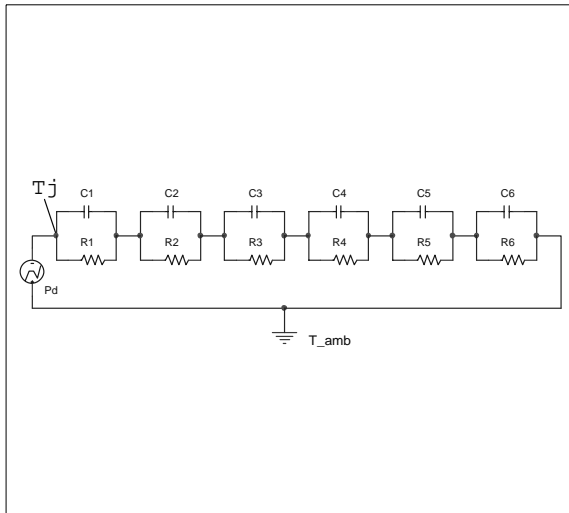
$R_{thj-amb}$ Vs. PCB copper area in open box free air condition



SO-16L Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in SO-16L



Pulse calculation formula

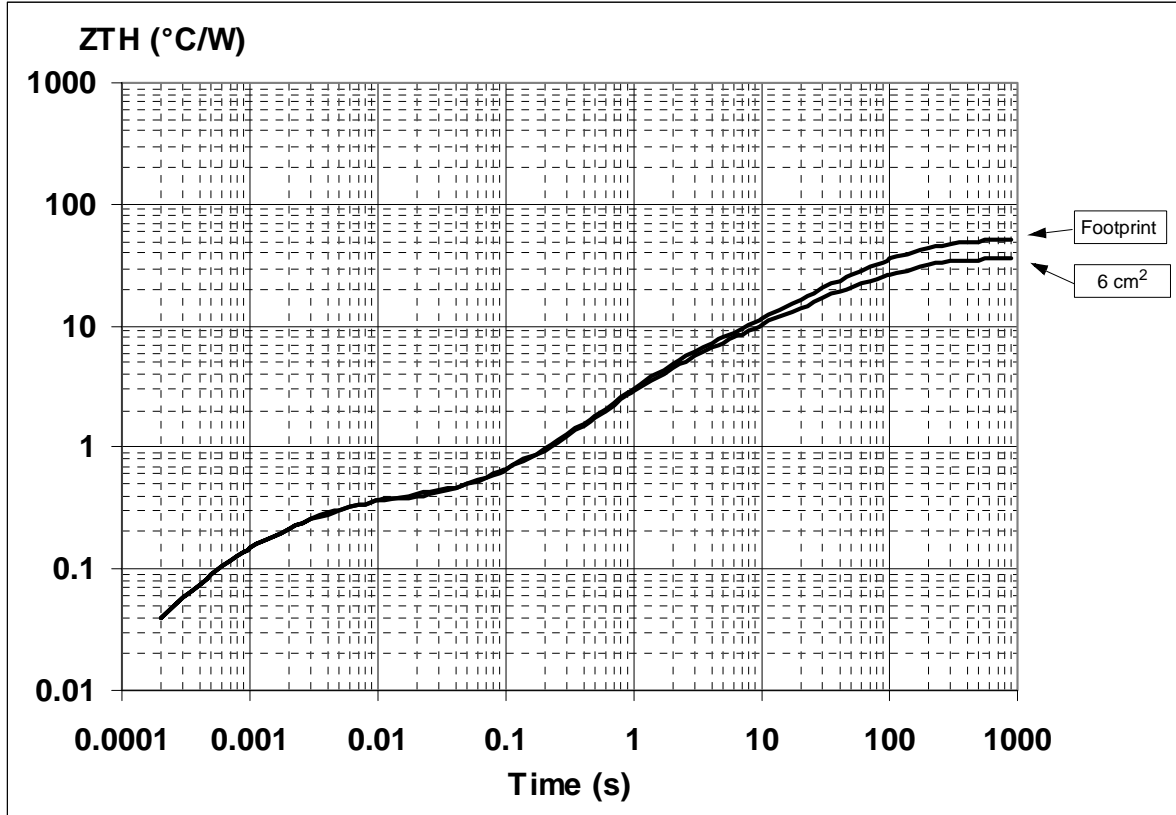
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

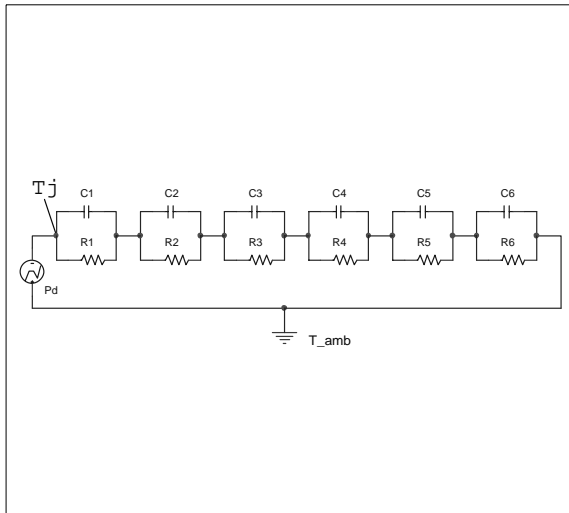
Thermal Parameter

| Area/island (cm^2) | Footprint | 6 |
|---|-----------|----|
| R1 ($^{\circ}\text{C}/\text{W}$) | 0.02 | |
| R2 ($^{\circ}\text{C}/\text{W}$) | 0.1 | |
| R3 ($^{\circ}\text{C}/\text{W}$) | 2.2 | |
| R4 ($^{\circ}\text{C}/\text{W}$) | 12 | |
| R5 ($^{\circ}\text{C}/\text{W}$) | 15 | |
| R6 ($^{\circ}\text{C}/\text{W}$) | 35 | 20 |
| C1 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.0015 | |
| C2 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 7.00E-03 | |
| C3 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 1.50E-02 | |
| C4 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 0.14 | |
| C5 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 1 | |
| C6 ($\text{W}\cdot\text{s}/^{\circ}\text{C}$) | 5 | 8 |

P²PAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in P²PAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

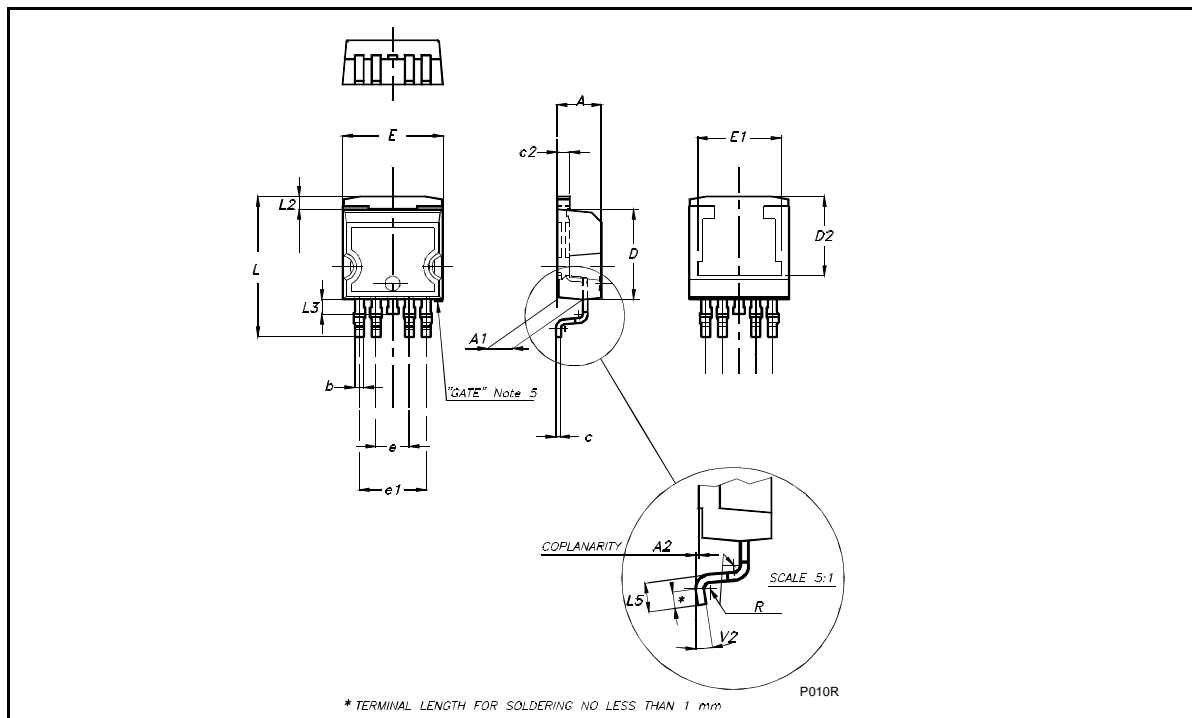
where $\delta = t_p/T$

Thermal Parameter

| Area/island (cm ²) | Footprint | 6 |
|--------------------------------|-----------|----|
| R1 (°C/W) | 0.02 | |
| R2 (°C/W) | 0.1 | |
| R3 (°C/W) | 0.22 | |
| R4 (°C/W) | 4 | |
| R5 (°C/W) | 9 | |
| R6 (°C/W) | 37 | 22 |
| C1 (W.s/°C) | 0.0015 | |
| C2 (W.s/°C) | 0.007 | |
| C3 (W.s/°C) | 0.015 | |
| C4 (W.s/°C) | 0.4 | |
| C5 (W.s/°C) | 2 | |
| C6 (W.s/°C) | 3 | 5 |

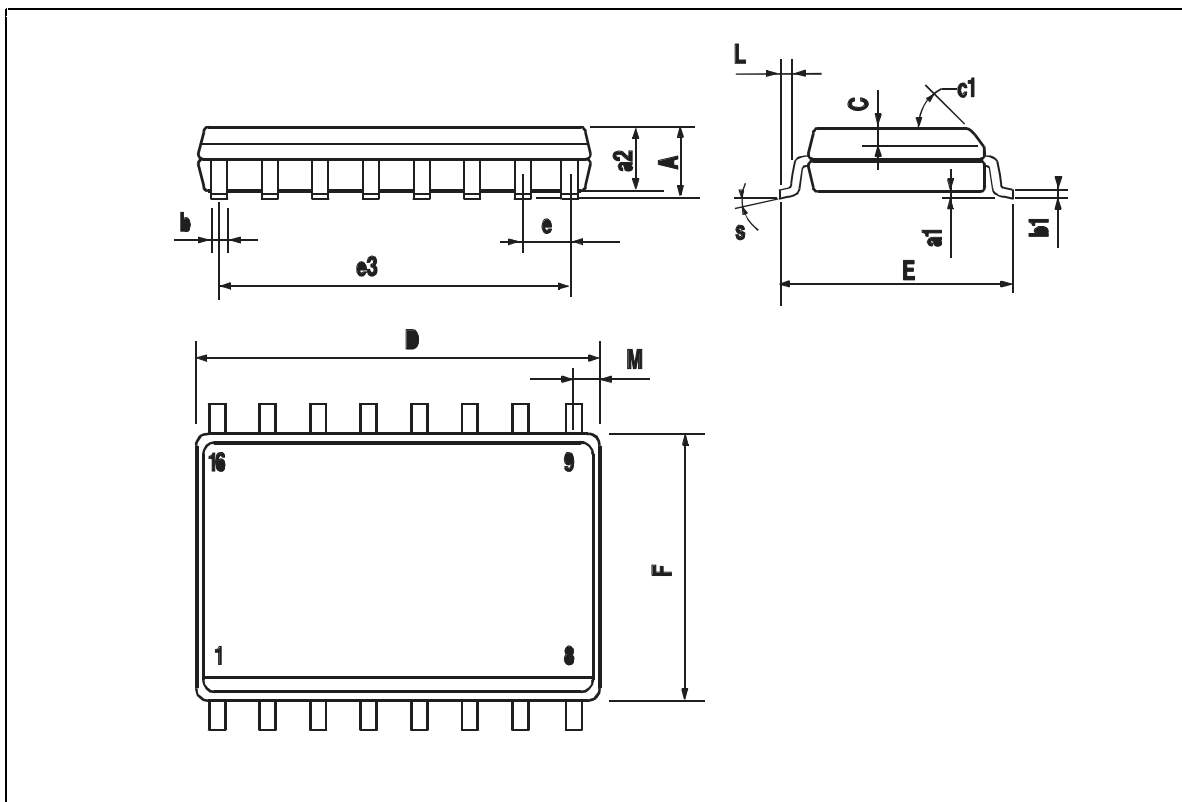
P²PAK MECHANICAL DATA

| DIM. | mm. | | |
|----------------|---------------|------|-------|
| | MIN. | TYP | MAX. |
| A | 4.30 | | 4.80 |
| A1 | 2.40 | | 2.80 |
| A2 | 0.03 | | 0.23 |
| b | 0.80 | | 1.05 |
| c | 0.45 | | 0.60 |
| c2 | 1.17 | | 1.37 |
| D | 8.95 | | 9.35 |
| D2 | | 8.00 | |
| E | 10.00 | | 10.40 |
| E1 | | 8.50 | |
| e | 3.20 | | 3.60 |
| e1 | 6.60 | | 7.00 |
| L | 13.70 | | 14.50 |
| L2 | 1.25 | | 1.40 |
| L3 | 0.90 | | 1.70 |
| L5 | 1.55 | | 2.40 |
| R | | 0.40 | |
| V2 | 0° | | 8° |
| Package Weight | 1.40 Gr (typ) | | |



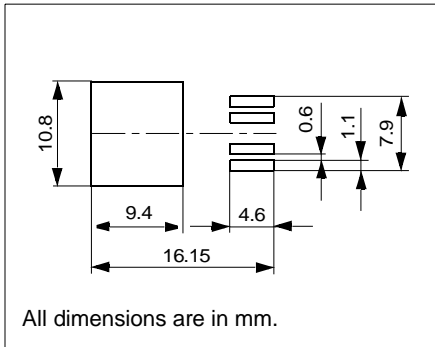
SO-16L MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------------|------|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 10.1 | | 10.5 | 0.397 | | 0.413 |
| E | 10.0 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.300 |
| L | 0.5 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |

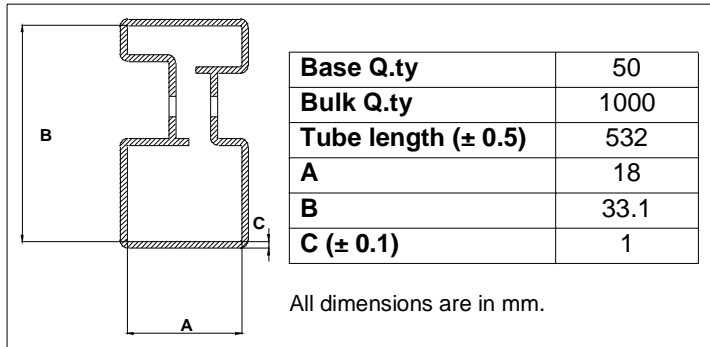


VN920D-B5 / VN920DSO

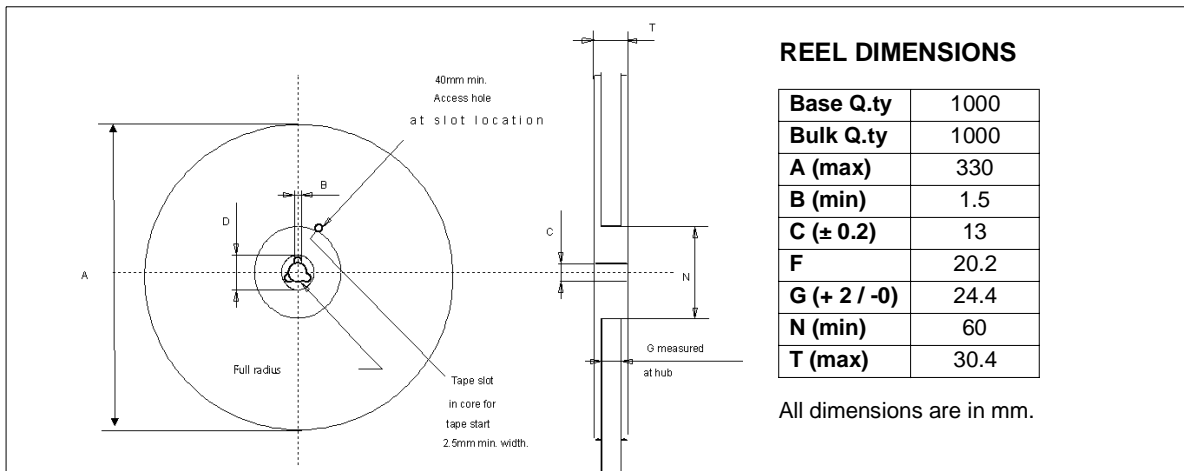
P²PAK SUGGESTED PAD LAYOUT



P²PAK TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

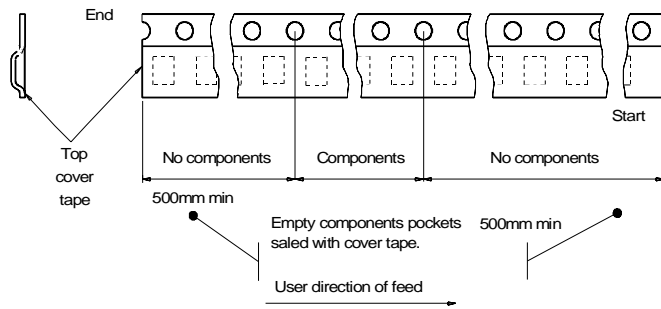
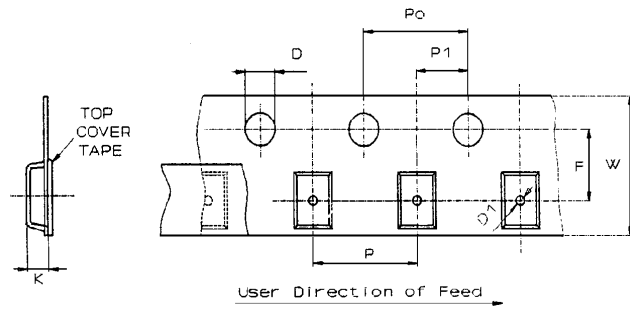
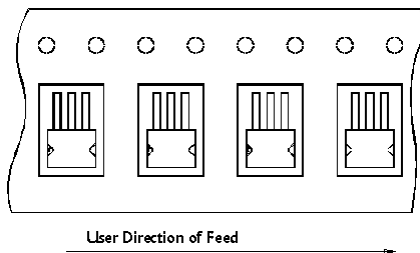


TAPE DIMENSIONS

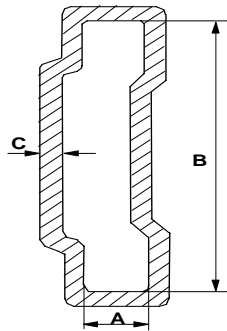
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|-------------------|--------------|------|
| Tape width | W | 24 |
| Tape Hole Spacing | P0 (± 0.1) | 4 |
| Component Spacing | P | 16 |
| Hole Diameter | D (± 0.1/-0) | 1.5 |
| Hole Diameter | D1 (min) | 1.5 |
| Hole Position | F (± 0.05) | 11.5 |
| Compartment Depth | K (max) | 6.5 |
| Hole Spacing | P1 (± 0.1) | 2 |

All dimensions are in mm.



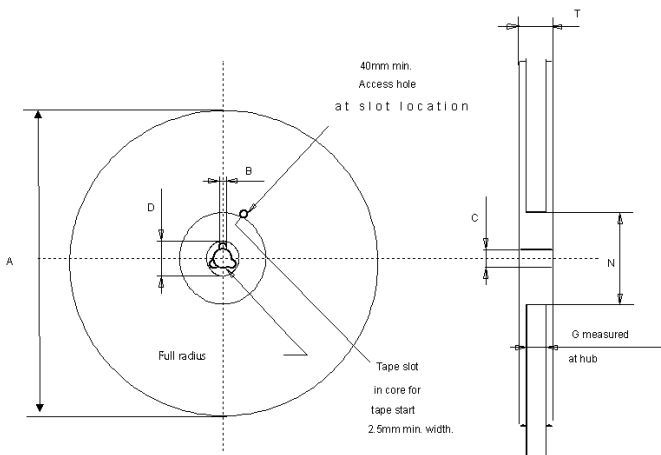
SO-16L TUBE SHIPMENT (no suffix)



| | |
|---|------|
| Base Q.ty | 50 |
| Bulk Q.ty | 1000 |
| Tube length (± 0.5) | 532 |
| A | 3.5 |
| B | 13.8 |
| C (± 0.1) | 0.6 |

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

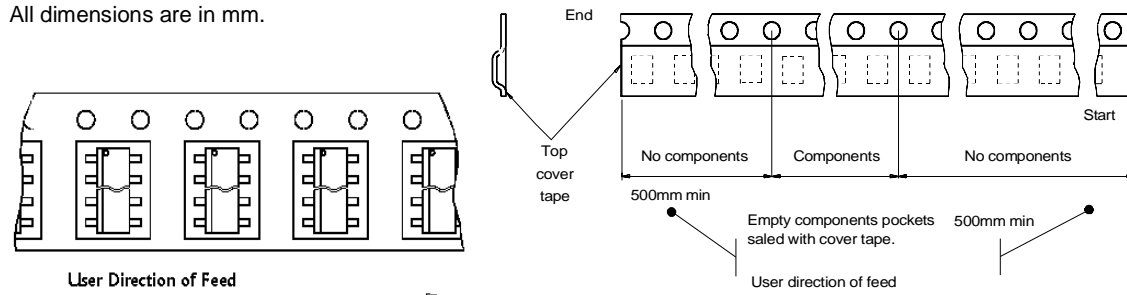
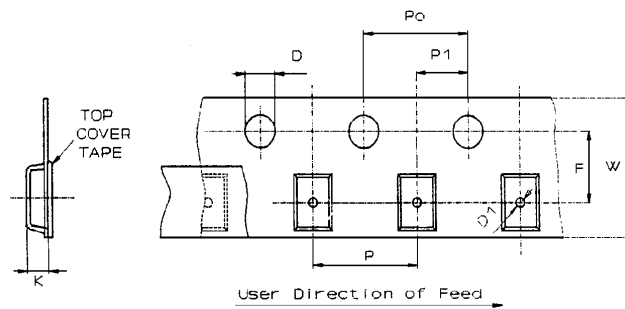
| | |
|---------------------------------|------|
| Base Q.ty | 1000 |
| Bulk Q.ty | 1000 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (± 0.2) | 13 |
| F | 20.2 |
| G (+ 2 / - 0) | 16.4 |
| N (min) | 60 |
| T (max) | 22.4 |

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|--------------------------|------------------------------------|-----|
| Tape width | W | 16 |
| Tape Hole Spacing | P0 (± 0.1) | 4 |
| Component Spacing | P | 12 |
| Hole Diameter | D ($\pm 0.1/-0$) | 1.5 |
| Hole Diameter | D1 (min) | 1.5 |
| Hole Position | F (± 0.05) | 7.5 |
| Compartment Depth | K (max) | 6.5 |
| Hole Spacing | P1 (± 0.1) | 2 |

All dimensions are in mm.



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